AU6850 Datasheet

USB Host MP3 Decoder SOC

Rev 1.0

Nov 24 , 2007

DISCLAIMER

All information and data contained in this document are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Any new issue of this document invalidates previous issues. Product availability and delivery are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, Shanghai Mountain View Silicon Technology Co. Ltd.("MVSILICON") does not assume responsibility for patent infringements or other rights of third parties that may result from its use.

Shanghai Mountain View Silicon Technology Co. Ltd. assumes no responsibility for any errors contained herein.

Revision History

Data	Revision	Description
2007-11-24	1.0	Initial release

Contents

Figures

Tables

1. Overview

A highly integrated SOC for MP3 player, AU6850 integrates MCU, MP3 decoder, USB Host controller, SD/MMC card controller, a 16-bit audio decoder and an IR decoder in a single chip. Besides AU6850 embedded a 32KB OTP memory, which provide an ultra low cost, low power consumption, flexible and more powerful Host MP3 player solution compared with other traditional flash-MP3 player.

1.1 Features

- Low power 0.18um CMOS technology
- Power supply 1.8V/3.3V, power consumption 80mW
- Enhanced 8051, up to 10 times faster than standard 8051
- Dynamic MCU running clock frequency adjustment to reduce power consumption and EMI
- USB2.0 full-speed host controller
- SD/MMC card controller
- Support MPEG 1/2/2.5 layer3 decoding, data rate 32kbps ~ 320kbps, including VBR
- Support 9 sampling frequency: 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 16-bit sigma-delta audio DAC
- Embedded headphone amplifier
- Support IR Remote control
- GPIO for various purposes
- Embedded 32KB OTP memory for program code storage
- Support external NOR flash for program code storage (AU6850A only)
- Support in-system debug through external emulator (AU6850A only)

1.2 Chip Architecture

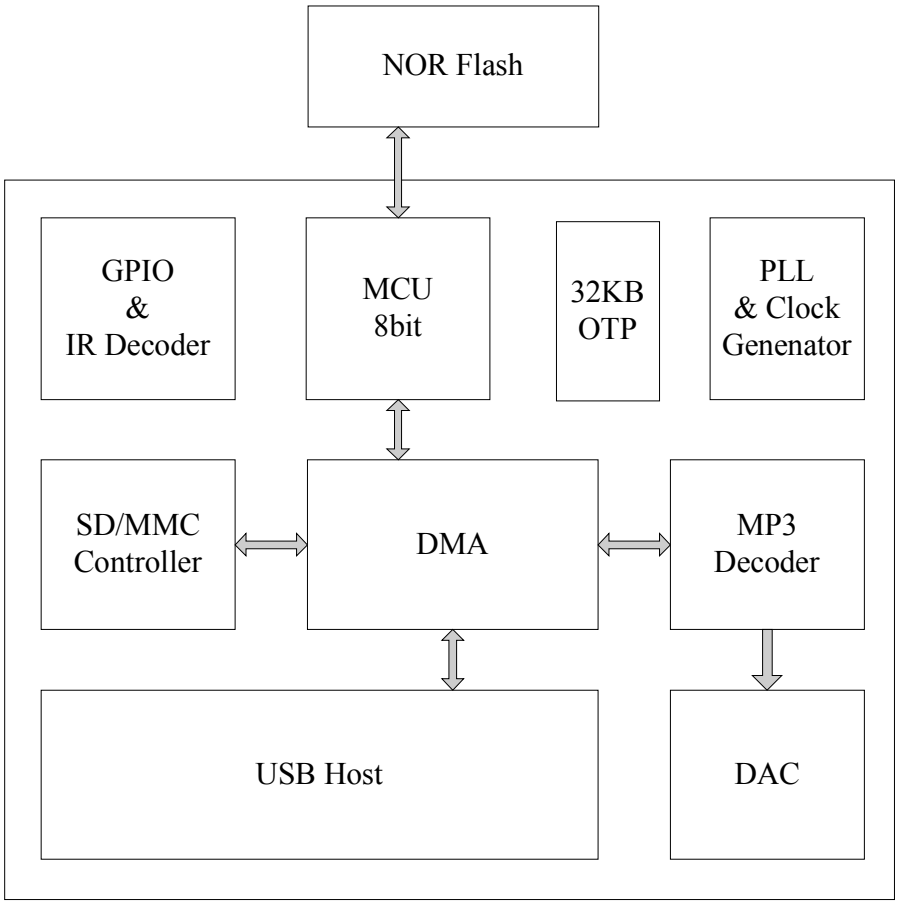

Figure 1 AU6850A Functional Block Diagram

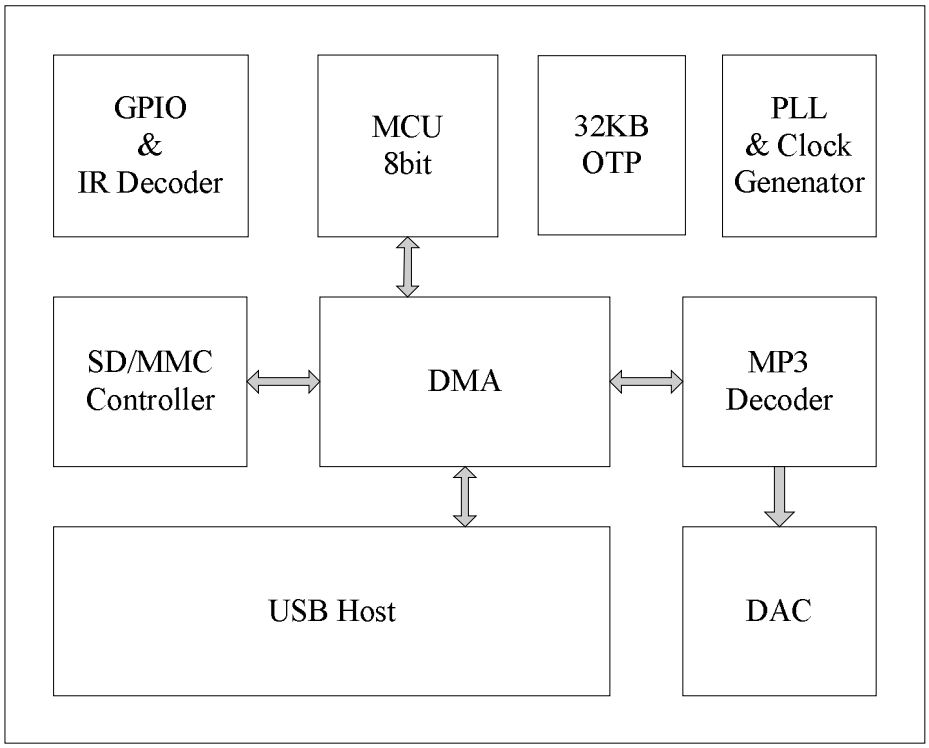

Figure 2 AU6850 Functional Block Diagram

2. System Application

• MP3 mini audio system

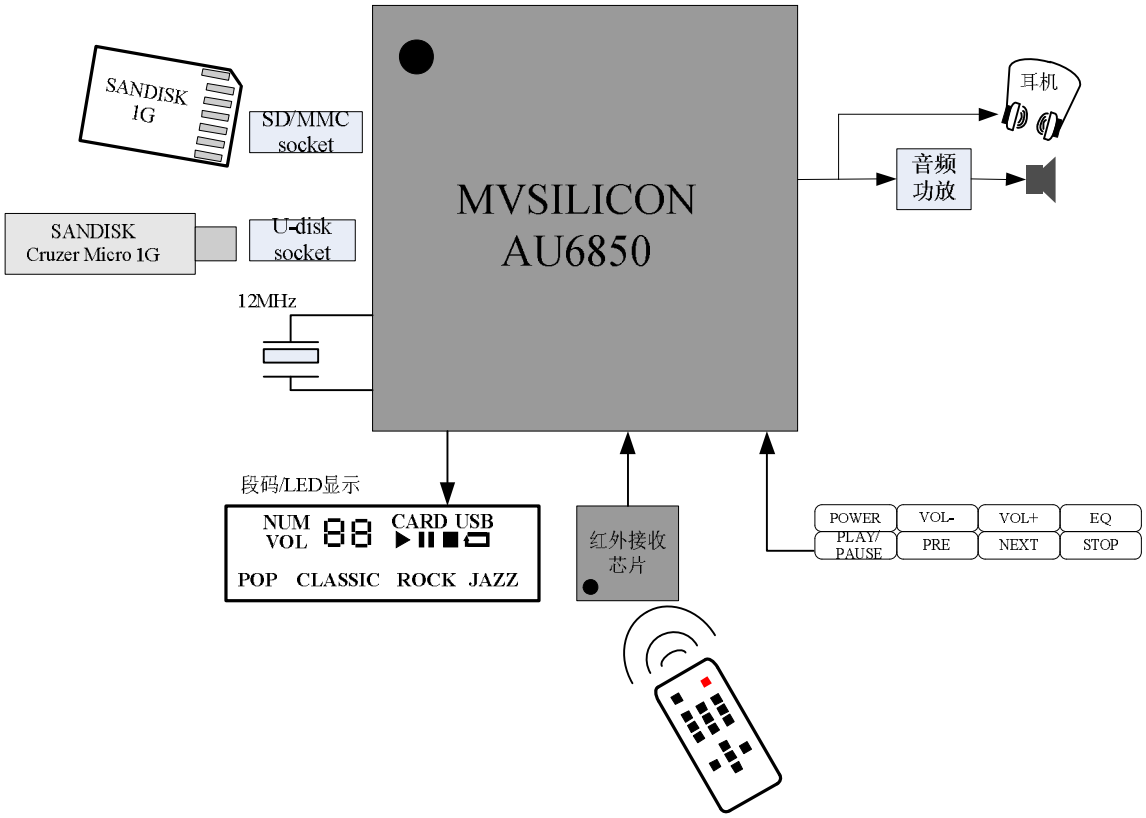

Figure 3 MP3 Mini Audio System

3. Pin Description

AU6850A/AU6850 is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
I/OD	Bidirectional, Open drain output
AI	Analog Input
AO	Analog Output
PWR	Power
GND	Ground

3.1 AU6850A Pin Description

Table 1 AU6850A Pin Description

Pin name	Pin #	Type	Description
			NOR flash memory interface pins
FSH_DB [7:6]	17:18	I/O	Flash memory data bus
FSH_DB [5:2]	22:25	I/O	Flash memory data bus
FSH_DB [1:0]	32:33	I/O	Flash memory data bus
FSH_AB[15:14]	61:62	I/O	Flash memory address bus
FSH_AB[13]	64	I/O	Flash memory address bus
FSH_AB[12]	60	I/O	Flash memory address bus
FSH_AB[11]	68	I/O	Flash memory address bus
FSH_AB[10]	43	I/O	Flash memory address bus
FSH_AB[9]	67	I/O	Flash memory address bus
FSH_AB[8]	65	I/O	Flash memory address bus
FSH_AB[7:6]	54:53	I/O	Flash memory address bus
FSH_AB[5:4]	44:45	I/O	Flash memory address bus
FSH_AB[3:1]	35:37	I/O	Flash memory address bus
FSH_AB[0]	42	I/O	Flash memory address bus
			USB interface pins
DP	49	I/O	USB Function D+ bus
DM	48	I/O	USB Function D- bus

			CARD interface pins
SD_CLK	56	O	SD Card clock
SD_CMD	58	I/O	SD Card command line
SD_DAT	59	I/O	SD Card data line
			Remote control pin
IR	21	I	Inferred remote controller signal
			DAC AUDIO interface pins
HPOUTL	4	AO	Head phone left channel output
HPOUTR	1	AO	Head phone right channel output
VREF	7	AO	Internal voltage reference
			GPIO/MCU IO pins
P1[7:3]	88:84	I/OD	MCU P1 PORT
P1[2:0]	71:69	I/OD	MCU P1 PORT
P0[1]	16	I/OD	MCU P0 PORT, can used as RXD
P0[0]	15	I/OD	MCU P0 PORT, can used as TXD
GP_A[7:4]	79:76	I/O	GPIO Bank A PORT
GP_A[3:2]	73:72	I/O	GPIO Bank A PORT
GP_A[1:0]	52:51	I/O	GPIO Bank A PORT
GP_B[7:4]	41:38	I/O	GPIO Bank B PORT
GP_B[3:0]	29:26	I/O	GPIO Bank B PORT
			CLK & Reset pins
XIN	11	I	Crystal oscillator input for PLL
XOUT	12	O	Crystal oscillator output for PLL
RESETn	20	I	System reset, active low
			Debug pin
DEBUG	93	I	When tied high, chip enter into debug mode and use external emulator. When tie low, chip works in normal mode
EXROM	94	I	When tied high, chip use external flash as MCU program code rom. When tie low, chip use internal OTP as MCU program code rom.
			Power/Ground pins
AVDD33	5 6	PWR	Analog power for DAC(3.3V)
AVSS	3 2	GND	Analog ground for DAC
PLL_AVSS	8	GND	Analog ground for PLL
PLL_AVDD18	9	PWR	Analog power for PLL(1.8V)
VDD33	13 34 50 55 74 92	PWR	Digital power for I/O(3.3V)
VSS	19 30 47 57 66 81	GND	Digital IO/core ground
VDD18	10	PWR	Digital power for core (1.8V)

	31 46 63 80		
Reserved	100:95 91:89 83:82 75 14	NC	Don't used, leave them floating

3.2 AU6850 Pin Description

Table 2 AU6850 Pin Description

Pin name	Pin #	Type	Description
			USB interface pins
DP	31	I/O	USB Function D+ bus
DM	30	I/O	USB Function D- bus
			CARD interface pins
SD_CLK	36	O	SD Card clock
SD_CMD	38	I/O	SD Card command line
SD_DAT	39	I/O	SD Card data line
			Remote control pin
IR	16	I	Inferred remote controller signal
			DAC AUDIO interface pins
HPOUTL	3	AO	Headphone left channel output
HPOUTR	1	AO	Headphone right channel output
VREF	5	AO	Internal voltage reference
			GPIO/MCU IO pins
P1[7:3]	59:55	I/OD	MCU P1 PORT
P1[2:0]	44:42	I/OD	MCU P1 PORT
P0[1]	13	I/OD	MCU P0 PORT, can used as RXD
P0[0]	12	I/OD	MCU P0 PORT, can used as TXD
GP_A[7:4]	52:49	I/O	GPIO Bank A PORT
GP_A[3:2]	46:45	I/O	GPIO Bank A PORT
GP_A[1:0]	34:33	I/O	GPIO Bank A PORT
GP_B[7:4]	27:24	I/O	GPIO Bank B PORT
GP_B[3:0]	20:17	I/O	GPIO Bank B PORT
			CLK & Reset pins
XIN	9	I	Crystal oscillator input for PLL
XOUT	10	O	Crystal oscillator output for PLL
RESETn	15	I	System reset, active low
			Power/Ground pins
AVDD33	4	PWR	Analog power for DAC(3.3V)
AVSS	2	GND	Analog ground for DAC

PLL_AVSS	6	GND	Analog ground for PLL
PLL_AVDD18	7	PWR	Analog power for PLL(1.8V)
VDD33	11 23 32 35 47 60	PWR	Digital power for I/O(3.3V)
VSS	14 21 29 37 41 54	GND	Digital IO/core ground
VDD18	8 22 28 40 53	PWR	Digital power for core (1.8V)
Reserved	64:61 48	NC	Don't used, leave them floating

4. Package

4.1 Package Diagram

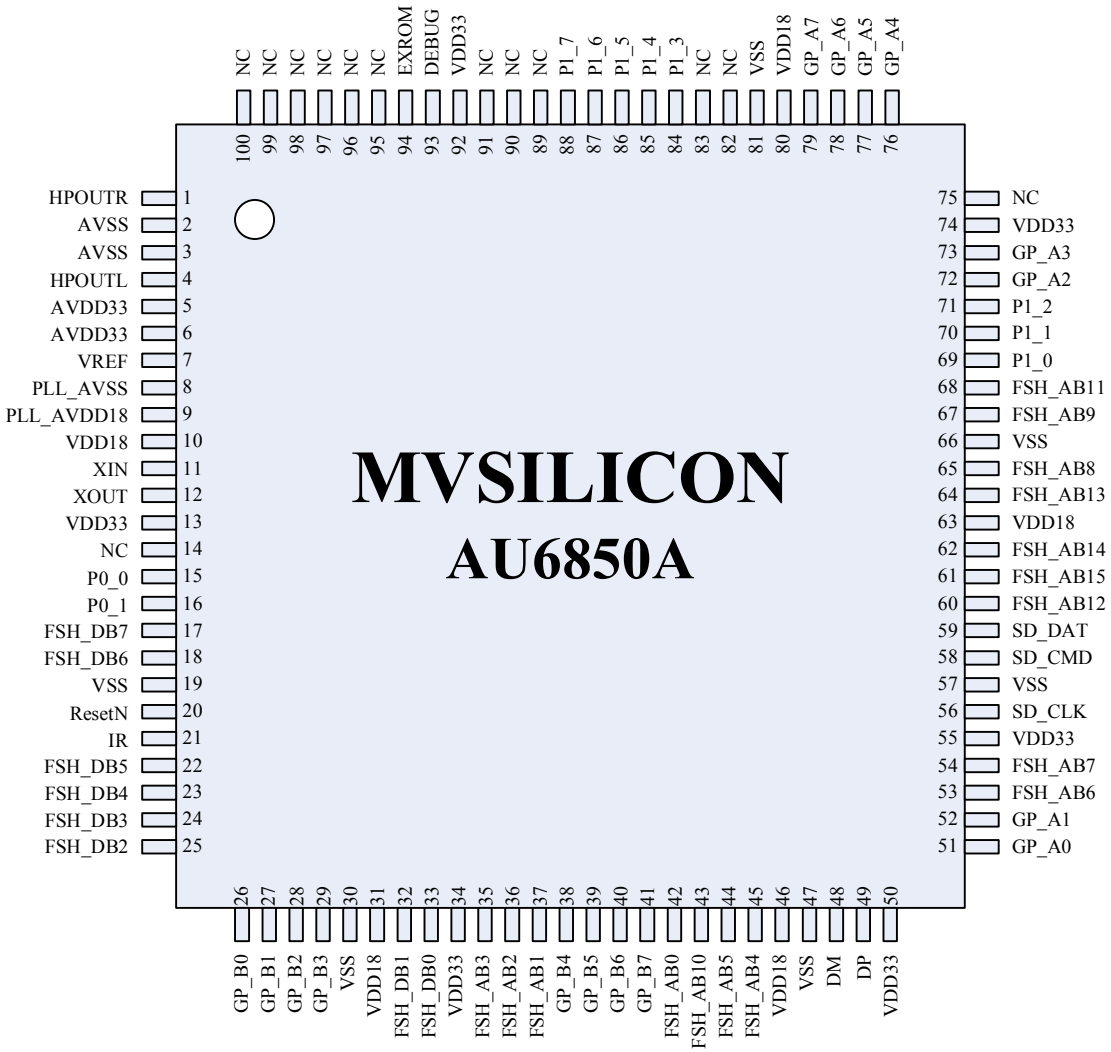

Figure 4 AU6850A Package Diagram (LQFP100-14x14mm / TOP View)

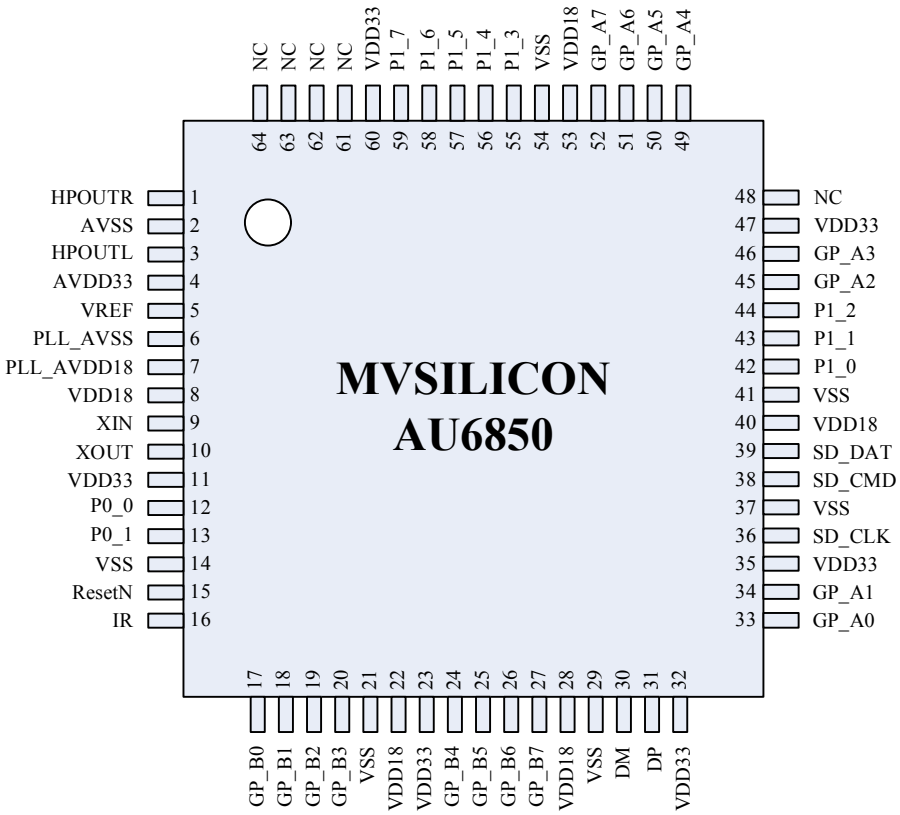

Figure 5 AU6850 Package Diagram (LQFP64-10x10mm / TOP View)

Notes: The “NC” IO in these diagrams means “not connected”, please leave them floating.

4.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.50BSC		
L	0.40	0.60	0.80
L1	1.00BSC		
θ	0	—	8°

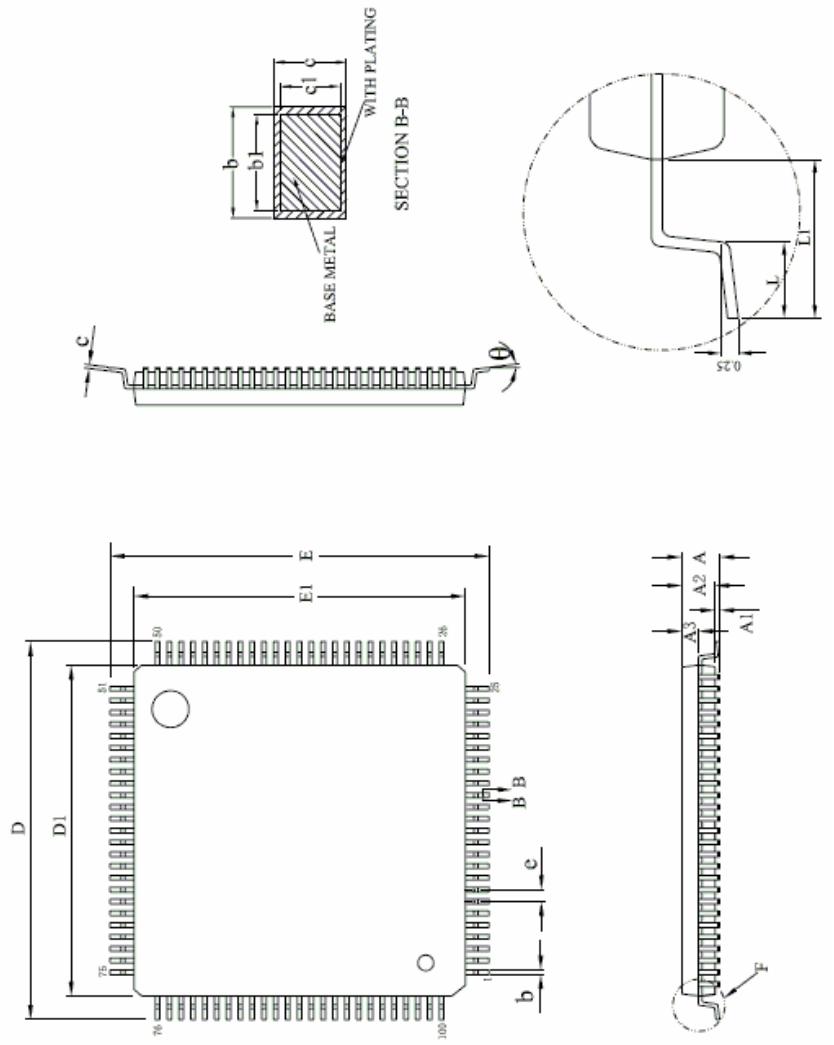

Figure 6 LQFP100-14x14mm Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

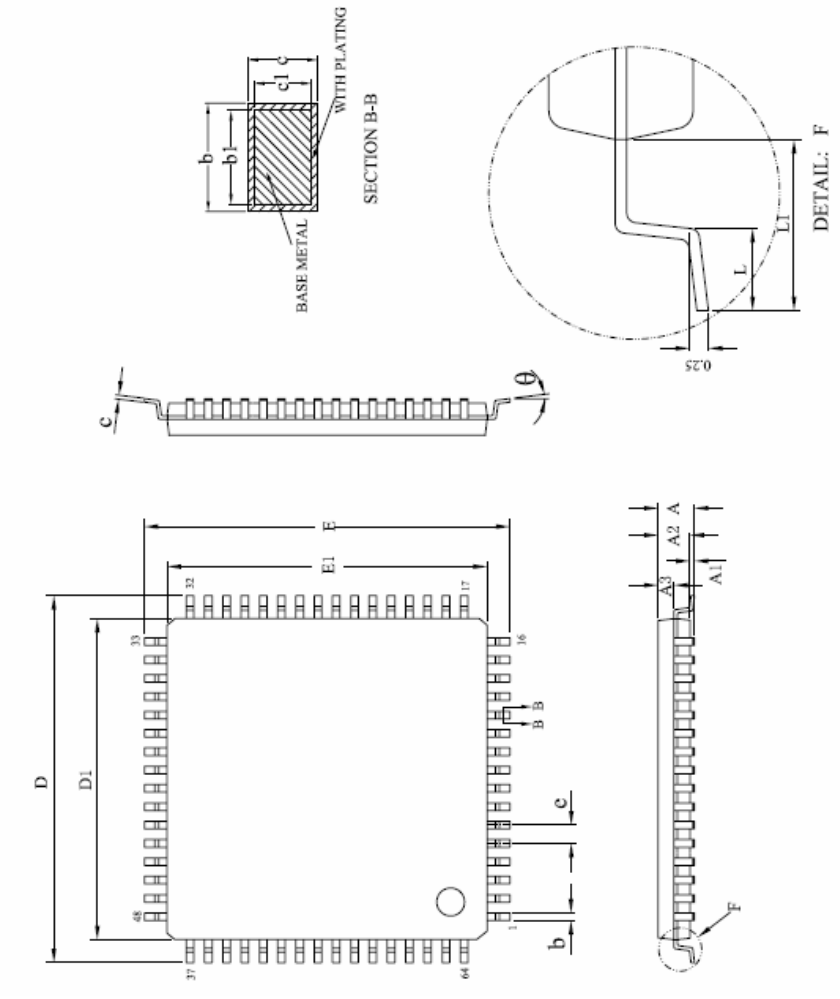

Figure 7 LQFP64-10x10mm Package Dimension Parameter

5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCC_IO_AB	-0.5 to 4.6	V
Power Supply Voltage (Core)	VCC_CORE_AB	0 to 2	V
Power Supply Voltage (PLL)	VCC_PLL_AB	-0.2 to 2.2	V
Power Supply Voltage (DAC)	VCC_DAC_AB	-0.3 to 3.6	V
Storage Temperature	TEMP_STG	-65 to 150	C

5.2 Recommended Operating Conditions

Table 4 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (IO)	VCC_IO_OP	3.0	3.3	3.6	V
Power Supply Voltage (Core)	VCC_CORE_OP	1.62	1.8	1.98	V
Power Supply Voltage (PLL)	VCC_PLL_OP	1.62	1.8	1.98	V
Power Supply Voltage (DAC)	VCC_DAC_OP	3.0	3.3	3.6	V
Input Voltage (digital)	VIN	0		3.6	V
Operating Temperature	TEMP_OPR	0		70	C

5.3 Electrical Characteristics

Table 5 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		2.0		3.6	V
VIL	Input Low Voltage		0		0.8	V
VOH	Output high voltage	@IOH=2mA	2.4			V
VOL	Output low voltage	@IOL=2mA			0.4	V
IOL	Low level output current for 8mA pins	@VOL = 0.4V	9.4	15.9	19.8	mA
IOH	Low level output current for 8mA pins	@VOH = 2.4V	11.2	23.8	38.3	mA
IL	Input leakage current		-10		10	uA
IOZ	Tri-state output leakage current		-10		10	uA
P_PLAY	Power consumption when playing	Playing mode		80		mW

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Contact Information

Shanghai Mountain View Silicon Technology Co Ltd

Shanghai Headquarter:
Suite 403, Jinying Tower A, 1518 Minsheng Road, Pudong New Area,
Shanghai, P.R. China
Zip code: 200135
Tel: 86-21-68549851
Fax: 86-21-68549859

Shenzhen Sales & Technical Support Office:
Suite 8C Olympic Plaza, Shangbao Road, Futian District,
Shenzhen, Guangdong, P.R. China
Zip code: 518034
Tel: 86-755-83522955
Fax: 86-755-83522957

Email: support@mvsilicon.com
Website: http://www.mvsilicon.com